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09/996,279	11/28/2001	Lothar Risch	L&L-I0178	4049

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EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 03/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/996,279	RISCH ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/17/04*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *03/18/04*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

Applicants' amendment faxed on December 18, 203 has been entered on January 13, 2004 .

Therefore claims 1-20 as recited in the Supplemental amendment are currently pending in the Application.

Claims 20-25 have been cancelled.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 4-20 rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (U.S. Patent No. 6,365,465, herein after Chang) in view of Burghartz et al. (U.S. Patent No. 5,461,250, herein after Burghartz) both previously Applied (for response to Applicants' arguments see section below).

With respect to claim 1, Chang discloses a method of fabricating a double gate MOSFET, including the steps in the following sequence :

Providing a substrate having a silicon substrate layer (Fig. 1 A # 4, col. 4 lines 5-6); a first insulation layer disposed on the silicon substrate layer (Fig. 1 A # 3, col. 4 line

7); a first spacer layer disposed on the first insulation layer (Fig. 1 A #11); and a semiconductor layer disposed on the first spacer layer (fig. 1 A # 5): patterning the semiconductor layer resulting in a semiconductor layer structure provided as a channel of the double gate MOSFET (fig. 1 A #5, channel between s/d 9); depositing a second spacer layer on the semiconductor layer and the first spacer layer (fig. 3 A # 2);

It is noted that the limitation " in the following sequence" it is noted that :

"Generally , Applicants' reversed order of process sequence as compared to the applied references including Chan , can not be considered as an act of invention, since reversing the order of prior art process step is held to render prima facie Obvious"

Ex Parte Rubin, 126 USPQ 440 (BAPI, 1959).

Further , " As a matter of fact selection of any order of performing process steps is prima fcie obvious in absence of new or unexpected results. "

In re Burhaus, 154 F.2d. 690, 69 USPQ 330 (CCPA 1946).

Therefore the sequence of performing the steps does not patentably distinguish the presently recited claim over the applied prior art.

Applicants' have added the phrase, " for producing gates aligned accurately with one another" in the preamble of the claim .

It is noted that the recitation, "for producing gates aligned accurately with one another" has not be given patentable weight because it has been held that a preamble is denied the effect of a limitation .." Kropa V Robie , 88 USPQ 478 (CCPA 1951).

Chang does not specifically disclose the step of completely embedding the semiconductor structure in the first and second separation layers by patterning the first and second spacer layers.

However, Burghartz in figures1, 2 and col. 6 lines 4 to7 describe completely embedding the semiconductor structure in the first and second separation layers by patterning the first and second separtionr layers to decrease interface scattering and providing a region of high mobility charge carriers as near the gate as possible to maximize the capacitance and enhance device performance.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Burkhart's step of completely embedding the semiconductor structure in the first and second spacer layers by patterning the first and second spacer layers in Chang's method to decrease interface scattering and providing a region of high mobility charge carriers as near the gate as possible to maximize the capacitance and enhance device performance. (Burghartz col. 2 lines 60-65).

The remaining limitations of claim 1 are:

depositing a second insulation layer on the structure formed of the first and second spacer layers (fig. 3A # 7): vertically etching two depressions disposed along one direction, the two depressions dimensioned such that the semiconductor layer structure is situated completely between them: during the etching of the two depressions, the second insulation layer, the first and second separation layers and, in each case on both sides, an edge section of the semiconductor layer structure being etched through completely in each case; filling the depressions with electrically

conductive material (fig. 3 C # 17), forming aregion of the separation layers extending from the contact hole to the smeicondcutor layer structure and in which region the semicodncutor layer structure is embedded in the separation layers by etching the region of the separation layers through the contact hole (fig. 1 D); applying a third insulation layers on inner walls of a region of removed separation layers and on surfaces of the semiconductor layer structure (figs. 20 to 2Q) and introducing a further electrically conductive material into the region of the removed separation layers. (2Y # 12).

With respect to claim 2, wherein the substrate structure is formed by applying the first insulation layer, the first separation layer, and the semiconductor layer one after another. (See claim1 above. It is noted that current case law is , "As a matter of fact selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results. In re Burhaus, 154 F.2d 690, 69 USPQ330 (CCPA 1946, therefore without a showing of criticality or unexpected results the recited order of steps is prima facie obvious).

With respect to claim 4, wherein the forming the substrate includes the steps of :

Providing the silicon substrate functioning as a first semiconductor substrate (fig. 1A # 4); applying the first insulation layer on the first semiconductor substrate (Fig. 1 A # 3, col. 4 line 7); providing a second semiconductor substrate (Fig. 1 a # 12); applying the first separation layer on the second semiconductor substrate (fig. 1A # 11); connecting the first and second semiconductor substrates to one another using a wafer bonding process between the insulation layer and the first separation layer (Figs. 2A to 2C, col. 4 lines 46-61) and reducing a thickness of the second semiconductor substrate resulting in the semiconductor layer (col. 4 lines 58-60, boron etch).

With respect to claim 5, wherein the first and second separation layers are formed from silicon nitride (fig. 2 F layers # 2 & 7).

With respect to claim 6, wherein the second insulating layer is planarized after being deposited.(fig. 2G and col. 6 lines 64-66).

With respect to claim 7, wherein the step of selectively removing the first and second separation layers through the contact hole made in the second insulation layer.(fig. 2G).

With respect to claims 8 and 13, wherein the electrically conductive material is formed from a material selected from the group consisting of doped polycrystalline silicon, metal and silicide. (col. 6 lines 15-18).

With respect to claims 9 and 14, wherein the doped polycrystalline silicon is formed by Chemical Vapor phase deposition and a doping is performed during deposition. (col. 4 lines 27-29).

With respect to claim 10, the method comprises " selectively removing the first and second separation layers by wet-chemical etching .(col. 6 lines 1-5).

With respect to claim 11, the method comprises applying the third insulation layers using a thermal oxidation process. (col. 6 line 10).

With respect to claim 12, wherein the step of producing a relatively thin oxide layer on the surface of the semiconductor layer structure and producing a relatively thick oxide layer on the inner walls of the region of the removed separation layers. (figs. 2C and 2 T , col. 4 lines 47-49 and col. 6 lines 9-14).

With respect to claim 15, wherein an oxide layer is applied as the first insulation layer (fig. 1 A).

With respect to claim 16, wherein a silicon layer is applied as the semiconductor layer(col. 6 line 15-17).

With respect to claim 17, wherein an oxide is deposited as the second insulation layer. (fig. 2G).

With respect to claim 18, wherein an oxide layer is applied as the third insulation layer.(fig. 2G).

With respect to claim 19, wherein arsenic atoms are used in the doping process. (col. 7 line 43)

With respect to claim 20, wherein phosphorous atoms are used in the doping process.(col. 7 line 44).

B. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (U.S. Patent No. 6,365,465, herein after Chan) as applied to claims 1-2 above, and further in view of Shimizu (U.S. Patent No. 5,753,541, herein after Shimizu).

With respect to claim 3, wherein the step of recrystallizing the semiconductor layer after being applied by being irradiated with a laser beam.

Chang does not specifically describe the step of recrystallizing the semiconductor layer after being applied by being irradiated with a laser beam.

However, Shimizu, a patent from the same filed of endeavor, describes in col. 5 lines 33-38 describes the step of recrystallizing the semiconductor layer after being applied by being irradiated with a laser beam to make the substrate a semi conductive layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to include Shimizu's laser annealing step(i.e. recrystallizing the semiconductor layer after being applied by being irradiated with a laser beam to make the substrate a semi conductive layer) in Chang's method so that further processing steps can use lower temperature than conventional methods wherein polycrystalline material is used. (Shimizu col. 3 lines 59-63).

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been fully considered but are not persuasive because :

Applicants' first contention that" the Examiner has not shown and articulated sufficient teaching, motivation , or suggestion in the prior art and particularly in the primary Chan reference for combining Chan and Burghartz as proposed" is trying to create new law/rules.

The examiner has shown prima facie obviousness by combining the secondary reference Burghartz with the primary reference Chan and the motivation provided in the secondary and not the other way around (as stated by the Applicants).

(a) It has clearly be shown above and admitted to by the Applicants' (present response page 19 lines 1-4 , etc.) that the motivation to combine Chan and Burghartz has been shown without having to refer to hindsight reconstruction (Applicants' contention that the Previous Office Action did not provide the motivation to combine the references is not entirely understood because the previous O/A page 5 line 2 (Burhartz col. 2 lines 60-65) and page 8 lines 2nd last line Shimizu col. 3 lines 59-63) provides more than enough motivation to combine the references.) .

(b) it is also the present law that , " there is no requirement that a motivation to make modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. *In re McLaughlin, 170 USPQ209 (CCPA1969).*

Applicants' next contention that their method of performing the steps results in the alleged new and advantageous result " very accurate alignment " is not persuasive because in scaled devices very accurate alignment is essential in order to achieve the

desired performance of devices and this very accurate alignment is neither new nor unexpected.

For reasons stated above and incorporated here by reference prima facie case of obviousness has been established by the combined teachings of Chan and Shimizu.

Therefore all of applicants' arguments are not persuasive.

Therefore all pending claims are finally rejected.

In accordance with Applicants' request The Examiner contacted Mr. Don Paris ( ) on March 15, 16, 2004 , and Mr. Werner Stemer on march 18, 2004 to see if claim language could be agreed to make them allowable. Mr. Paris faxed a copy of the proposed amendment to the Examiner. However Mr. Paris left a message on March 17, 2004 that his clients cannot agree to the proposed amendment and want a Final rejection. (Mr. Werner Stemer on 03/18/2004) .

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H. Rao whose telephone number is (703) 306-5945. The examiner can normally be reached on Monday- Friday from approximately 7:00 a.m. to 5:30 p.m.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7722.

Steven H. Rao

Patent Examiner

March 16, 2004.

SPE 2814